ABSTRACT OF THE DISCLOSURE

A processor includes a first circuit and a second circuit. The first circuit is configured to provide a first indication of whether or not at least one reservation is valid in the processor. A reservation is established responsive to processing a load-linked instruction, which is a load instruction that is architecturally defined to establish the reservation. A valid reservation is indicative that one or more bytes indicated by the target address of the load-linked instruction have not been updated since the reservation was established. The second circuit is coupled to receive the first indication. Responsive to the first indication indicating no valid reservation, the first circuit is configured to select a speculative load-linked instruction for issued. The second circuit is configured not to select the speculative load-linked instruction for issue responsive to the first indication indicating the at least one valid reservation. A method is also contemplated.